

What is Claimed is:

1 1. In a test and debug system in which a target
2 processor transmits trace data to a host processing unit;
3 apparatus for transferring the data from the target
4 processor comprising:

5 a trace packet unit, the trace packet unit
6 reformatting trace packets into export trace packets; and

7 a flush packet unit, the flush packet unit generating
8 a flush export trace packet when the trace packet unit does
9 not have sufficient data to generate a trace export packet.

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11 2. Apparatus as recited in claim 1 wherein the flush
12 packet unit is activated in response to a halt signal
13 during a non-interruptible code segment.

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15 3. Apparatus as recited in claim 2 further
16 comprising a storage unit, the storage unit storing a first
17 signal in response to the halt signal, the first signal
18 activating the flush packet unit.

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20 4. Apparatus as recited in claim 3 wherein the first
21 signal is removed when code execution resumes.

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23 5. Apparatus as recited in claim 4 further
24 comprising:

1 an export unit for transmitting export trace packets
2 to the host processing unit; and

3 a switch, the switch determining whether an export
4 trace packet or a flush export trace packet is applied to
5 the export unit.

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7 6. The method of generating export trace packets,
8 the method comprising:

9 reformatting trace packets into export trace packets;
10 and

11 generating a flush export trace packet when the data
12 from the trace packets do not provide a complete export
13 trace packet.

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15 7. The method as recited in claim 6 wherein the
16 flush export trace packet is generated after a halt signal
17 is generated during execution of a non-interruptible code
18 segment.

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20 8. The method as recited in claim 7 further
21 comprising:

22 storing a first signal in a storage unit as a result
23 of a halt signal, the halt signal controlling the
24 generation of the flush export trace packet.

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1 9. The method as recited in claim 8 wherein the
2 first signal is removed when the target processor begins
3 executing code.

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5 10. A target processor comprising:
6 a processing unit;
7 a trace unit, the trace unit coupled to the processing
8 unit, the trace unit gathering test and debug data from the
9 processing unit, the trace unit formatting the test and
10 debug data in trace packets; and

11 a trace export unit, the trace export unit including:
12 a trace packet unit for converting trace packets
13 to export trace packets; and
14 a flush packet unit for generating trace packets
15 when the converting a trace packet does not result in a
16 complete export trace packet.

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18 11. The target processor as recited in claim 10
19 wherein the flush packet unit is activated in response to a
20 halt signal during a non-interruptible code segment.

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22 12. The target processor as recited in claim 11
23 wherein the trace unit further includes a storage unit, the
24 halt signal resulting in a storage of a first signal in the
25 storage unit, the first signal activating the flush packet
26 unit.

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1 13. The target processor as recited in claim 12
2 wherein the trace unit further includes a switch, the
3 switch determining whether the trace packet unit or the
4 flush trace unit is transmitted to the host processing
5 unit.

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7 14. The target processor as recited in claim 13
8 wherein the first signal is removed from the storage unit
9 when the processor begins code execution.